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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/576,177	04/19/2006	Yoshinari Higaki	0553-0494	7224

26568 7590 06/16/2009

COOK ALEX LTD
SUITE 2850
200 WEST ADAMS STREET
CHICAGO, IL 60606

EXAMINER	
WONG, TINA MEI SENG	

ART UNIT	PAPER NUMBER
2874	

MAIL DATE	DELIVERY MODE
06/16/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/576,177	HIGAKI ET AL.	
	Examiner	Art Unit	
	TINA M. WONG	2874	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6* is/are allowed.

6)☒ Claim(s) *1-5 and 7-14* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 13 May 2009 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 and 7-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,323,051 to Shimada in view of U.S. Patent 7,071,037 to Suzawa et al.

In regards to claim 1, Shimada teaches a semiconductor device (Figure 1d) comprising a transparent conductive film (6) and a plurality of thin film transistors (21) over a substrate (1) having an insulating surface (3) and an electrode or a wiring formed by stacking a second conductive layer (2') on the first conductive layer (2) wherein the first conductive layer has a larger width that the second conductive layer and wherein the transparent conductive film is on a part of the first conductive film extending from an end portion of the second conductive layer. But Shimada fails to teach a semiconductor thin film over the substrate and a first conductive layer in contact with the semiconductor thin film. However, Suzawa et al teaches an additional

semiconductor thin film layer (505/1001) over a substrate and in contact with a first conductive layer. Additionally, Suzawa et al teaches the semiconductor layer to be formed in order to etch the desired tapered angles. Suzawa et al further teaches the semiconductor layer to be formed by a sputter method, the same method Shimada teaches to form the first and second conductive layers. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have included an additional semiconductor thin film in the arrangement claimed by Applicant for the reasons discussed in Suzawa et al.

In regards to claim 2, Shimada teaches a semiconductor device (Figure 1d) comprising a transparent conductive film (6) and a plurality of thin film transistors (21) over a substrate (1) having an insulating surface (3) and an electrode or a wiring formed by stacking a second conductive layer (2') on the first conductive layer (2) wherein the first conductive layer has a portion projected from an end portion of the second conductive layer, and wherein the transparent conductive film is on the portion of the first conductive film projected from the end portion of the second conductive layer. But Shimada fails to teach a semiconductor thin film over the substrate and a first conductive layer in contact with the semiconductor thin film. However, Suzawa et al teaches an additional semiconductor thin film layer (505/1001) over a substrate and in contact with a first conductive layer. Additionally, Suzawa et al teaches the semiconductor layer to be formed in order to etch the desired tapered angles. Suzawa et al further teaches the semiconductor layer to be formed by a sputter method, the same method Shimada teaches to form the first and second conductive layers. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have

included an additional semiconductor thin film in the arrangement claimed by Applicant for the reasons discussed in Suzawa et al.

In regards to claims 3-5, Shimada teaches a semiconductor device (Figure 1d) comprising a transparent conductive film (6) and a plurality of thin film transistors (21) having an insulating surface (3) and an electrode or a wiring formed by stacking a second conductive layer (2') on the first conductive layer (2) wherein a side surface portion of the first conductive layer has the same tapered angle as a side surface portion of the second conductive layer, and wherein the transparent conductive film is on the side surface portion of the first conductive layer. But Shimada fails to teach a semiconductor thin film over the substrate and a first conductive layer in contact with the semiconductor thin film. However, Suzawa et al teaches an additional semiconductor thin film layer (505/1001) over a substrate and in contact with a first conductive layer. Additionally, Suzawa et al teaches the semiconductor layer to be formed in order to etch the desired tapered angles. Suzawa et al further teaches the semiconductor layer to be formed by a sputter method, the same method Shimada teaches to form the first and second conductive layers. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have included an additional semiconductor thin film in the arrangement claimed by Applicant for the reasons discussed in Suzawa et al.

Furthermore, Shimada fails to explicitly teach for the side surface portion of the first conductive layer to have a smaller or larger tapered angle than a side surface portion of the second conductive layer. However, Applicant claims a taper of the same, smaller and larger angle between the two conductive layers. Since Applicant claims multiple tapered angle possibilities and states for each of the tapered angles to be capable of performing with a

reasonably equivalently in the semiconductor device, this limitation is a non-critical aspect of the invention. Since Shimada shows the same tapered angle between the two layers and since Applicant claims the three tapered angles to function equivalently, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have chosen any one of the three tapered angles.

In regards to claim 7, Shimada teaches the first conductive layer to be formed with titanium, molybdenum, alloy containing titanium or ally containing molybdenum.

In regards to claim 8, Shimada teaches the second conductive layer to be formed with aluminum or alloy containing aluminum.

In regards to claim 9, Shimada teaches a light emitting element in which the transparent conductive film serves as an anode or a cathode.

In regards to claim 10, Shimada teaches a liquid crystal element in which the transparent conductive film to serve as pixel electrodes (26).

In regards to claim 11, Shimada teaches the transparent conductive film to be formed with ITO or IZO.

In regards to claim 12, Shimada teaches a surface of the second conductive layer covered with an oxide film.

In regards to claim 13, although Shimada teaches the first and second conductive film to be formed continuously in the same sputter apparatus, the limitation is a method limitation in a device claim. Applicant is claiming a product, not a method of manufacturing the product. The patent being sought in the preceding claims is an end product that is met by the previously applied reference.

In regards to claim 14, Shimada teaches the semiconductor device to be used in a mobile information terminal, a video camera, a digital camera or a personal computer.

Allowable Subject Matter

Claim 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record fails to disclose or reasonably suggest a flattening insulating layer having a contact hole over the semiconductor film and the electrode/wiring formed over the flattening insulating film to be in contact with the semiconductor thin film through the contact hole in addition to the accompanying features of the independent claim and the intervening claims.

Claim 6 is allowed. The prior art of record fails to disclose or reasonably suggest a flattening insulating layer having a contact hole over the semiconductor film and the electrode/wiring formed over the flattening insulating film to be in contact with the semiconductor thin film through the contact hole in addition to the accompanying features of the independent claim.

Response to Arguments

Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TINA M. WONG whose telephone number is (571)272-2352. The examiner can normally be reached on Monday-Friday 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Uyen-Chau Le can be reached on (571) 272-2397. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tina M Wong/
Primary Examiner, Art Unit 2874